UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,986	09/19/2005	Norio Sakai	36856.1370	3417

54066 7590 10/08/2008

MURATA MANUFACTURING COMPANY, LTD.
C/O KEATING & BENNETT, LLP
1800 Alexander Bell Drive
SUITE 200
Reston, VA 20191

EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
10/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JKEATING@KBIPLAW.COM
uspto@kbiplaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/549,986	SAKAI ET AL.	
	Examiner	Art Unit	
	HUNG VU	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-30* is/are pending in the application.

4a) Of the above claim(s) *30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on 09/12/08 has been entered. An action on the RCE follows.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 23-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Wermer et al. (WO 02/19430, of record).

Regarding claim 23, Wermer et al. discloses, as shown in Figures 3 and 4, a ceramic multilayer substrate comprising:

a ceramic laminate (90) including a plurality of ceramic layers, having a first main surface (upper surface of layer 91), and including internal circuit elements (141,143 and vias) disposed inside of the laminate;

a resin layer (80) having a bonding surface (lower surface of 3) in contact with the first main surface of the ceramic laminate and a mounting surface (upper surface of 10) opposite to the bonding surface;

external electrodes (101,121,125,116), each disposed on the mounting surface of the resin layer and electrically connected to at least one of the internal circuit elements of the ceramic laminate;

a ground electrode (125, on the right) disposed inside of the resin layer;

the ground electrode is arranged to overlap at least one of the external electrodes (116, on the right) in a direction of lamination of the plurality of ceramic layers.

Regarding claim 24, Wermer et al. discloses the ground electrode includes a metal that is integral with the ceramic laminate [Figures 3-4].
Note that the terms "laminate", "sintered" and "baked" are method recitations in a device claimed.

Regarding claim 25, Wermer et al. discloses the substrate further comprising a first circuit component (105) mounted on the first main surface and covered with the resin layer, wherein the ground electrode (125, on the right and on the left) is disposed on a side that is closer to the mounting surface than the first circuit component [Figures 3-4].

Regarding claim 26, Wermer et al. discloses the first circuit component is disposed within a region defined by projecting the ground electrode on the first main surface [Figures 3-4].

Regarding claim 27, Wermer et al. discloses the substrate further comprising relay electrodes (107,111,113) disposed so as to extend along the first main surface, wherein electrical connection from the external electrodes to the internal circuit elements are provided through the relay electrodes [Figures 3-4].

Claims 23-27 are rejected under 35 U.S.C. 102(a) as being anticipated by Hirabayashi et al. (US 2004/0066617).

Regarding claim 23, Hirabayashi et al. discloses, as shown in Figures 6-19, a ceramic multilayer substrate comprising:

a ceramic laminate (4) including a plurality of ceramic layers, having a first main surface (4a), and including internal circuit elements (11 and vias) disposed inside of the laminate;

a resin layer (6,32) having a bonding surface in contact with the first main surface of the ceramic laminate and a mounting surface (2b) opposite to the bonding surface;

external electrodes (9), each disposed on the mounting surface of the resin layer and electrically connected to at least one of the internal circuit elements of the ceramic laminate;

a ground electrode (15a) disposed inside of the resin layer;

the ground electrode is arranged to overlap at least one of the external electrodes (9) in a direction of lamination of the plurality of ceramic layers.

Regarding claim 24, Hirabayashi et al. discloses the ground electrode includes a metal that is integral with the ceramic laminate [Figures 6-19].
Note that the terms "laminate", "sintered" and "baked" are method recitations in a device claimed.

Regarding claim 25, Hirabayashi et al. discloses the substrate further comprising a first circuit component (14) mounted on the first main surface and covered with the resin layer, wherein the ground electrode (15a) is disposed on a side that is closer to the mounting surface than the first circuit component [Figures 6-19].

Regarding claim 26, Hirabayashi et al. discloses the first circuit component is disposed within a region defined by projecting the ground electrode on the first main surface [Figures 6-19].

Regarding claim 27, Hirabayashi et al. discloses the substrate further comprising relay electrodes (13,15b) disposed so as to extend along the first main surface, wherein electrical connection from the external electrodes to the internal circuit elements are provided through the relay electrodes [Figures 6-19].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wermer et al. (WO 02/19430, of record) in view of Takehara et al. (US 2003/0071350, of record). Regarding claim 28, Wermer et al. discloses the claimed invention including the substrate as explained in the rejection above. Wermer et al. further discloses a substrate comprises a second main surface on an opposite side to the first main surface (bottom surface of 90). Wermer et al. does not disclose a second circuit component is mounted on the second main surface. However, Takehara et al. discloses a ceramic laminate (2) comprises a second main surface (upper surface of 2) on an opposite side to a first main surface (lower surface of 2) and a second circuit component (3) is mounted on the second main surface [Figures 1-9]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate of Wermer et al. further comprising a second circuit component mounting on the second main surface, such as taught by Takehara et a. in order to integrate more circuit components and to increase the circuit density.

Regarding claim 29, Wermer et al. and Takehara et al. disclose the claimed invention including the substrate as explained in the rejection above. Wermer et al. and Takehara et al. do not disclose a conductive case is disposed on the second main surface to cover the second circuit component. However, as shown in Figure 10, Takehara et al. discloses a conductive case (10) is disposed on a second main surface of a substrate (2) to cover the second circuit components (1,3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to form the substrate of Wermer et al. and Takehara et al. having a conductive case being disposed on the second main surface to cover the second circuit component, such as taught by Figure 10 of Takehara et al., in order to protect the circuit component from external contamination.

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi et al. (US 2004/0066617) in view of Takehara et al. (US 2003/0071350, of record). Regarding claim 28, Hirabayashi et al. discloses the claimed invention including the substrate as explained in the rejection above. Hirabayashi et al. further discloses a substrate comprises a second main surface on an opposite side to the first main surface (bottom surface of 4). Hirabayashi et al. does not disclose a second circuit component is mounted on the second main surface. However, Takehara et al. discloses a ceramic laminate (2) comprises a second main surface (upper surface of 2) on an opposite side to a first main surface (lower surface of 2) and a second circuit component (3) is mounted on the second main surface [Figures 1-9]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate of Hirabayashi et al. further comprising a second circuit component mounting on the second main surface, such as taught by Takehara et a. in order to integrate more circuit components and to increase the circuit density.

Regarding claim 29, Hirabayashi et al. and Takehara et al. disclose the claimed invention including the substrate as explained in the rejection above. Hirabayashi et al. and Takehara et al. do not disclose a conductive case is disposed on the second main surface to cover the second

circuit component. However, as shown in Figure 10, Takehara et al. discloses a conductive case (10) is disposed on a second main surface of a substrate (2) to cover the second circuit components (1,3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate of Hirabayashi et al. and Takehara et al. having a conductive case being disposed on the second main surface to cover the second circuit component, such as taught by Figure 10 of Takehara et al., in order to protect the circuit component from external contamination.

Response to Arguments

Applicant's arguments with respect to claim 23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Monday to Thursday 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272 - 1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vu

September 26, 2008

/Hung Vu/

Primary Examiner